intersil™

HSP50210

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Digital Costas Loop

The Digital Costas Loop (DCL) performs many of the baseband processing tasks required for the demodulation of BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM waveforms. These tasks include matched filtering, carrier tracking, symbol synchronization, AGC, and soft decision slicing. The DCL is designed for use with the HSP50110 Digital Quadrature Tuner to provide a two chip solution for digital down conversion and demodulation.

The DCL processes the in-phase (I) and quadrature (Q) components of a baseband signal which have been digitized to 10 bits. As shown in the block diagram, the main signal path consists of a complex multiplier, selectable matched filters, gain multipliers, cartesian-to-polar converter, and soft decision slicer. The complex multiplier mixes the I and Q inputs with the output of a quadrature NCO. Following the mix function, selectable matched filters are provided which perform integrate and dump or root raised cosine filtering (α = 0.40). The matched filter output is routed to the slicer, which generates 3-bit soft decisions, and to the cartesian-to-polar converter, which generates the magnitude and phase terms required by the AGC and Carrier Tracking Loops.

The PLL system solution is completed by the HSP50210 error detectors and second order Loop Filters that provide carrier tracking and symbol synchronization signals. In applications where the DCL is used with the HSP50110, these control loops are closed through a serial interface between the two parts. To maintain the demodulator performance with varying signal power and SNR, an internal AGC loop is provided to establish an optimal signal level at the input to the slicer and to the cartesian-to-polar converter

Features

- Clock Rates Up to 52MHz
- Selectable Matched Filtering with Root Raised Cosine or Integrate and Dump Filter
- Second Order Carrier and Symbol Tracking Loop Filters
- Automatic Gain Control (AGC)
- Discriminator for FM/FSK Detection and Discriminator Aided Acquisition
- Swept Acquisition with Programmable Limits
- Lock Detector
- Data Quality and Signal Level Measurements
- Cartesian to Polar Converter
- 8-Bit Microprocessor Control - Status Interface
- Designed to work with the HSP50110 Digital Quadrature Tuner
- 84 Lead PLCC

Applications

- Satellite Receivers and Modems
- BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM Demodulators
- Digital Carrier Tracking
- Related Products: HSP50110 Digital Quadrature Tuner, D/A Converters HI5721, HI5731, HI5741
- HSP50110/210EVAL Digital Demod Evaluation Board

Block Diagram